REMARKS

In the outstanding Official Action claims 19, 22 and 25 were allowed, while claims 2, 6, 8, 9, 13, 14, 16 and 17 were deemed to be allowable if placed in independent form. Claims 1, 3-5, 7, 11, 12, 15, 18, 21, 23 and 24 were rejected under 35 U.S.C. §102(b) as being anticipated by Ito et al, for the reasons of record.

In response, independent claims 1 and 18, and claim 2, have been amended in order to more clearly and precisely define the instant invention in a manner which clearly distinguishes over the cited and applied references, and accordingly the allowable claims have not been placed in independent form at this time, pending a final determination of the patentability of the remaining claims.

As herein amended, independent claims 1 and 18 now more narrowly and precisely recite that the first reference source includes a transistor (50) and that this transistor has a control terminal connected in parallel with a control terminal of the primary current source, a first terminal connected directly to a first terminal of the primary current source, and a second terminal coupled to a first current input. It is respectfully submitted that these limitations are essentially similar to those of allowable claim 2, differing primarily in that the limitations to claims 1 and 18 are not so narrow as to define a particular type of transistor (i.e. a PMOS transistor) as is recited in claim 2.

Accordingly, it is respectfully submitted that independent claims 1 and 18, and the remaining rejected claims depending therefrom, are now in condition for allowance for the same reasons as pertain with respect to allowable claim 2. Additionally, whereas claims 1 and 18 do not recite the particular type of transistor employed, both of these claims do include an additional limitation, namely that a first terminal of the transistor (50) is connected directly to a first terminal of the primary currently source (41), a limitation which is clearly not met by Ito, wherein the corresponding terminals are clearly not connected directly together, since they are clearly connected to different voltage supply terminals and are additionally separated by the component 5a.

Finally, it is noted that claim 12 was objected to because the secondary current source is recited as including the second transistor 44, whereas the specification teaches that transistor 44 is part of the process sensitive resistor 49. In response, this objection is respectfully traversed, because although it is true that the transistor 44 is part of the process sensitive resistor 49, as shown and described, it is also true that the secondary current source includes the second transistor 44, because this transistor forms part of a current mirror within the secondary current source. Clearly, it is possible for a transistor to form both a part of a process sensitive resistor and also for this

component to be included within a larger circuit, namely the secondary current source circuit.

In view of the foregoing, it is respectfully submitted that the currently-pending claims are clearly patentably distinguishable over the cited and applied reference, and that objection to claim 12 has been overcome. Accordingly, allowance of the currently-pending claims is respectfully submitted to be justified at this time, and favorable consideration is earnestly solicited.

Respectfully submitted,

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